

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Yasutoshi AIBARA et al.

Appln. No.:

Filed: HERewith

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND  
IMAGING SYSTEM

\* \* \*

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Applicants wish to make of record the documents cited in  
prior Application No. 10/080,586 filed February 25, 2002,  
whether cited by Applicants or by the Patent Office. The  
documents are listed on the attached Form PTO-1449.

Respectfully submitted,

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April 5, 2004

<b>FORM PTO-1449</b>				<b>Atty. Docket No.</b> XA-9625A		<b>Appln. No.</b>	
<b><u>LIST OF DOCUMENTS CITED BY APPLICANT</u></b>							
				<b>Applicant</b> Yasutoshi AIBARA et al.			
				<b>Filing Date</b> HEREWITH		<b>Group</b>	
<b>U.S. PATENT DOCUMENTS</b>							
<b>Examiner Initial</b>		<b>Document Number</b>	<b>Date</b>	<b>Name</b>	<b>Class</b>	<b>Sub-class</b>	<b>Filing Date</b>
	AA	6,515,698	02/04/03	Sasaki et al.	348	231.6	
	AB	6,192,146	02/20/01	Abe	382	165	
	AC	5,748,235	05/05/98	Kondo et al.	348	222	
	AD	5,020,118	05/28/91	Sugiura	382	50	
	AE	5,309,183	05/03/94	Sasaki et al.	348	233	
	AF	5,867,285	02/02/99	Hirota et al.	358	522	
	AG	6,081,254	06/27/00	Tanaka et al.	345	154	
	AH						
	AI						
<b>FOREIGN PATENT DOCUMENTS</b>							
<b>Examiner Initial</b>		<b>Document Number</b>	<b>Date</b>	<b>Country</b>	<b>Class</b>	<b>Sub-class</b>	<b>Translation</b>
	AJ						
	AK						
	AL						
	AM						
	AN						
<b>OTHER</b> (including author, title, date, pertinent pages, etc.)							
	AO						
	AP						
	AQ						
<b>Examiner</b>				<b>Date Considered</b>			
<b>EXAMINER:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.							